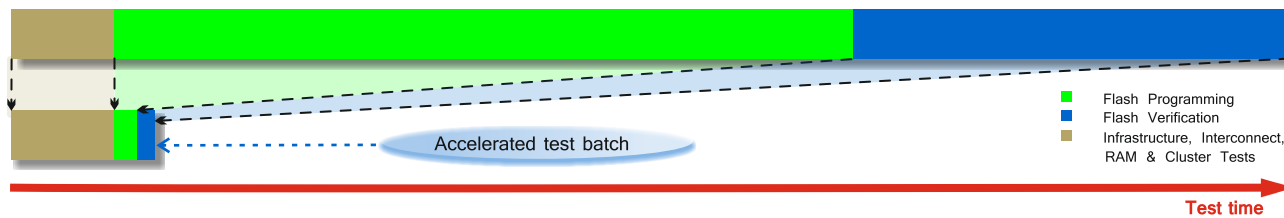


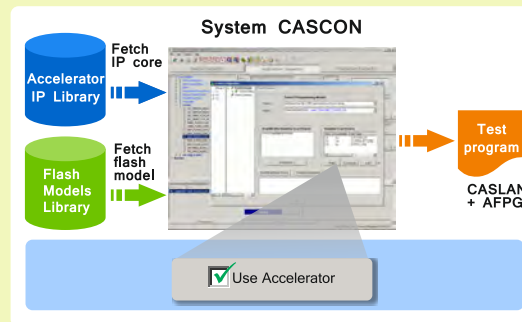
FPGA embedded ChipVORX® IP enables

TEST BATCH RUN TIME BREAKDOWN: Traditional vs. Accelerated



ChipVORX® Flash Accelerator IP library enables FPGA-based ultra fast in-system programming (ISP) of Flash via JTAG interface. The technology provides a speed increase in Flash configuration by loading specific IP into the FPGA that is connected to target Flash component. Typical acceleration for parallel Flash programming is in the range of **10x – 15x**, the factor for serial Flash goes up to **100x**. In many cases, the acceleration is only limited by the Flash internal programming speed. The usage of the IP does neither require expert background knowledge nor special FPGA design tools or programmer.

Integrated and automated solution



ChipVORX® Flash Accelerator technology is fully integrated into Goepel Electronic' SYSTEM CASCON™ software platform thus the recognition of connections between Flash target and FPGA as well as generation of flash programming test is done automatically.

Because of the ChipVORX® IP's independence of the target component to be programmed, the Flash type imposes no restrictions. In addition to serial Flash, parallel NOR and NAND Flash including bad block handling are supported.

As the same system libraries as for a "normal" Boundary Scan programming are used, users may update new Flash models by themselves.

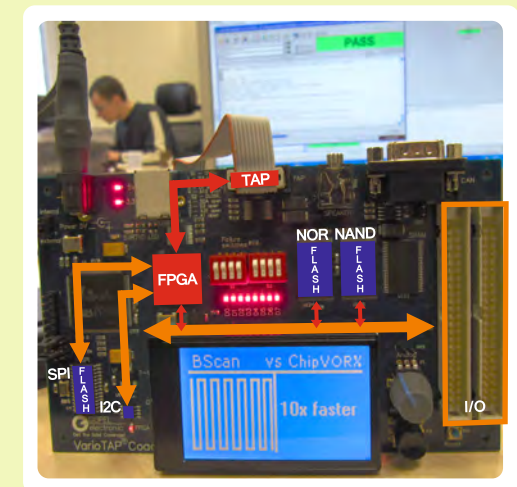
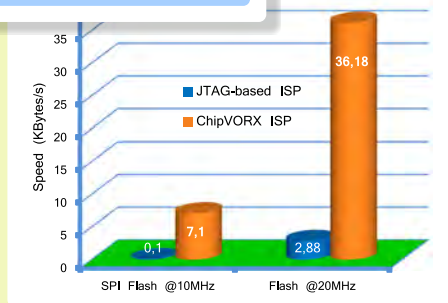
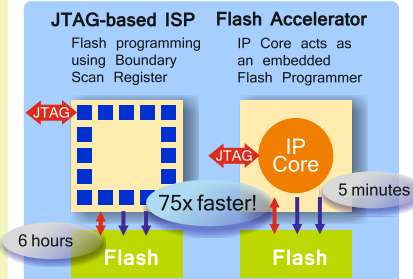
Existing Boundary Scan projects prepared using Goepel's SYSTEM CASCON™ toolsuite can be accelerated just by a single click on "Use Acceleration" checkbox.

Technology highlights

- Universal push-button solution: no extra engineering efforts
- Immediately speeds-up flash programming by **10-15 times**
- Up to **100x** acceleration for Flash memories with serial interface
- Support for all latest **Xilinx**, **Altera** and **Lattice** FPGAs
- Actel FPGAs are supported upon request
- Tightly integrated with Goepel's System **CASCON**
- Automated flash program generation (AFPG)
- Existing System **CASCON** test projects can be accelerated without re-engineering
- No FPGA design knowledge or third-party design tools required
- Full control over Flash programming process including communication protocol

Prerequisites

- Availability of FPGA device that is attached to the target flash IC
- System **CASCON™ 4.5.4** from Goepel Electronic
- Valid license for Flash ISP
- Valid **ChipVORX®** license



ultra fast Flash Programming

Supported FPGA devices

At the moment, the ChipVORX® models for Flash programming are available for all latest **Altera**, **Xilinx** and **Lattice** FPGA families, including **Spartan-3/A/E/AN**, **Spartan-6**, **Virtex-4**, **Virtex-5**, **Virtex-6**, **Cyclone**, **Cyclone II**, **Cyclone III**, **Cyclone IV**, **Stratix**, **Stratix II**, **Stratix III**, **Stratix IV**, **Arria GX**, **Arria II GX**, **LatticeXP**, **LatticeXP2**, **LatticeSC**, **LatticeECP/2/3**.

The support for Actel FPGAs as well as for older Xilinx, Altera and Lattice devices is also provided upon request.

Extra performance

If you need extra performance beyond the existing off-the-shelf ChipVORX® Flash Accelerator IP please request customized Flash Accelerator IP to achieve maximal possible Flash programming speed for a specific target board.

FPGA	FLASH TYPE	OPERATION	FLASH ACCELERATOR vs. JTAG-based ISP
Virtex 4 xc4vfx12	NOR	Program + Verify 1MB, 20 MHz	7.0x
	NOR	Program + Verify 1MB, 20 MHz	14.7x
Virtex 5 xc5vlx110t	SPI	Write + Read 32 KB, 10 MHz	74.6x
	NOR	Program + Verify 1MB, 20 MHz	3.7x
Spartan 3 xc3s50a	SPI	Write + Read 32 KB, 10 MHz	14.1x
	SPI	Write + Read 32 KB, 20 MHz	9.2x
	NOR	Program + Verify 1MB, 20 MHz	3.7x

Contacts

ChipVORX® Flash Accelerator IP library is actively developed by **Testonica Lab** in tight cooperation with **GOEPEL Electronic**. Testonica Lab is an official GATE program partner of **GOEPEL Electronic**.

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... and minutes into seconds

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